**Architecture Plan**

Admission system

**Contents**

[**List of table** 2](#_Toc389479200)

[**Revision** 3](#_Toc389479201)

[**1.** **Introduction** 4](#_Toc389479202)

[1.1. Purpose 4](#_Toc389479203)

[1.2. Goal 4](#_Toc389479204)

[**2.** **ACDM** 5](#_Toc389479205)

[2.1. ACDM 5](#_Toc389479206)

[2.2. ACDM Description 6](#_Toc389479207)

[2.2.1. Stage 1 6](#_Toc389479208)

[2.2.2. Stage 2 6](#_Toc389479209)

[2.2.3. Stage 3 7](#_Toc389479210)

[2.2.4. Stage 4 8](#_Toc389479211)

[2.2.5. Stage 5 9](#_Toc389479212)

[2.2.6. Stage 6 10](#_Toc389479213)

[2.2.7. Stage 7 11](#_Toc389479214)

[2.2.8. Stage 8 12](#_Toc389479215)

[**3.** **Architecture Schedule** 13](#_Toc389479216)

[**4.** **Role and Responsibilities** 14](#_Toc389479217)

[4.1. Responsibility 14](#_Toc389479218)

[4.1.1 Managing Engineer 14](#_Toc389479219)

[4.1.2 Chief Architect 14](#_Toc389479220)

[4.1.3 Requirement Engineer 15](#_Toc389479221)

[4.1.4 Chief Scientist 15](#_Toc389479222)

[4.1.5 Quality Process Engineer 16](#_Toc389479223)

[4.1.6 Support Engineer 16](#_Toc389479224)

[4.1.7 Production Engineer 17](#_Toc389479225)

[4.2. Role 17](#_Toc389479226)

# **List of table**

[Table 1: Revision history 3](#_Toc389479236)

[Table 2: Stage description 6](#_Toc389479237)

[Table 3: Stage 2 description 6](#_Toc389479238)

[Table 4: Stage 3 description 7](#_Toc389479239)

[Table 5: Stage 4 description 8](#_Toc389479240)

[Table 6: Stage 5 description 9](#_Toc389479241)

[Table 7: Stage 6 description 10](#_Toc389479242)

[Table 8: Stage 7 description 11](#_Toc389479243)

[Table 9: Stage 8 description 12](#_Toc389479244)

[Table 10: Architecture Schedule 13](#_Toc389479245)

[Table 11: Managing engineer responsibility 14](#_Toc389479246)

[Table 12: Chief Architect responsibility 14](#_Toc389479247)

[Table 13: Requirement Engineer responsibility 15](#_Toc389479248)

[Table 14: Chief Scientist responsibility 15](#_Toc389479249)

[Table 15: Quality Process Engineer responsibility 16](#_Toc389479250)

[Table 16: Support engineer responsibility 16](#_Toc389479251)

[Table 17: Product Engineer responsibility 17](#_Toc389479252)

[Table 18: Role 17](#_Toc389479253)

**List of figure**

[Figure 1: Architecture Process 5](#_Toc389478260)

# **Revision**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **No** | **Version** | **Update date** | **Author** | **Content** |
| 1 |  |  |  |  |
| 2 |  |  |  |  |

Table 1: Revision history

# **Introduction**

## Purpose

## Goal

# **ACDM**

## ACDM

Figure 1: Architecture Process

## ACDM Description

### Stage 1

|  |  |  |
| --- | --- | --- |
| **Steps** | **Process** | **Description** |
|  |  |  |

Table 2: Stage description

**Input:** N/A

**Output:**

### Stage 2

|  |  |  |
| --- | --- | --- |
| **Step** | **Process** | **Description** |
|  |  |  |

Table 3: Stage 2 description

**Input:**

**Output:**

### Stage 3

|  |  |  |
| --- | --- | --- |
| **Steps** | **Process** | **Description** |
|  |  |  |

Table 4: Stage 3 description

**Input:**

**Output:**

### Stage 4

|  |  |  |  |
| --- | --- | --- | --- |
| **Steps** | | **Process** | **Description** |
|  |  | |  |

Table 5: Stage 4 description

**Input:**

**Output:**

### Stage 5

|  |  |  |
| --- | --- | --- |
| **Steps** | **Process** | **Description** |
|  |  |  |

Table 6: Stage 5 description

**Input:**

**Output:**

### Stage 6

|  |  |  |
| --- | --- | --- |
| **Step** | **Process** | **Description** |
|  |  |  |

Table 7: Stage 6 description

**Input:**

**Output:**

### Stage 7

|  |  |  |
| --- | --- | --- |
| **Step** | **Process** | **Description** |
|  |  |  |

Table 8: Stage 7 description

**Input:**

**Output:**

### Stage 8

|  |  |  |
| --- | --- | --- |
| **Step** | **Process** | **Description** |
|  |  |  |

Table 9: Stage 8 description

**Input:**

**Output:**

# **Architecture Schedule**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Phase** | **Task name** | **Start** | **Finish** | **Resources name** |
| Architect & Design |  |  |  |  |
|  |  |  |  |

Table 10: Architecture Schedule

# **Role and Responsibilities**

## Responsibility

### Managing Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
|  |  |
|  |  |

Table 11: Managing engineer responsibility

### Chief Architect

|  |  |
| --- | --- |
| **Stage** | **Description** |
|  |  |
|  |  |

Table 12: Chief Architect responsibility

### Requirement Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
|  |  |
|  |  |

Table 13: Requirement Engineer responsibility

### Chief Scientist

|  |  |
| --- | --- |
| **Stage** | **Description** |
|  |  |
|  |  |

Table 14: Chief Scientist responsibility

### Quality Process Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
|  |  |
|  |  |

Table 15: Quality Process Engineer responsibility

### Support Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
|  |  |
|  |  |

Table 16: Support engineer responsibility

### Production Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
|  |  |
|  |  |

Table 17: Product Engineer responsibility

## Role

|  |  |  |
| --- | --- | --- |
| **No** | **Roles** | **Members applied** |
|  |  |  |
|  |  |  |

Table 18: Role